ESWAR COLLEGE OF ENGINEERING: NARASARAOPET

Approved by AICTE, New Delhi., Affiliated to JNTUK, Kakinada
Kesanupalli Village, Narasaraopet – 522 601,
Palnadu Dist. A.P.

Phone No. 9121214708 | Email ID: principal@eswarcollegeofengg.org, eswarcollegeofengg@gmail.com

web:eswarcollegeofengg.org

Department of Electronics and Communication Engineering

Dt: 4-7-2022

To
The Principal
Eswar College of Engineering
Narasaraopet

Through HOD-ECE

From
Shaik Mona
Assistant Professor
Faculty Coordinator

Sub: Requesting for permission to conduct a value-added course on **CMOS Digital VLSI Design** from **18-07-2022 to 23-07-2022.**

Dear Sir,

The Department of ECE is planning to organize a 1 week value-added course on **CMOS Digital VLSI Design** from **18-07-2022 to 23-07-2022.**

Total Number of Students registered: 106 No's (IV B.Tech I Sem ECE-A and B).

Resource Person: J Kavitha, Associate Professor, Department of ECE, St. Anns College of Engineering and Technology, Chirala.

Certificate Criteria: 60% of marks in Evaluation, 80% of attendance

In connection with the programme, we request your approval to organize the same and to make the programme a grand success.

Thanks and regards,

Name:,Shaik Mona

Signature

SHAIK MONA

HOD- Comments Please consider – K. Sandhya (HOD)

Department of ECE
Eswar College of Engineering
Kesanupalli (V), Narasaraopet - 522 601

Principal Comments: Recommended

Approved/ Rejected

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+91 99636 34414
Email: eswarcollegeofengg@gmail.com
Website: www.eswarcollegeofengg.org

Date: 11-07-2022

CIRCULAR

All B.Tech IV /I ECE students are hereby notified that a value added course titled "CMOS Digital VLSI Design" will be conducted from 18-07-2022 to 23-07-2022It is mandatory for all students to enroll their names with course co ordination SK Mona, Assistant Professor, Department of ECE.

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CONTENTS

- MOS TRANSISTOR BASIC-I, MOS TRANSISTOR BASIC-I,
- MOS TRANSISTOR BASIC-II, MOS PARASITIC & SPICE MODEL, CMOS INVERTER BASICS-I
- CMOS INVERTER BASICS-II, CMOS INVERTER BASICS-III.
- POWER ANALYSIS-I, POWER ANALYSIS-II, SPICE SIMULATION-I
- SPICE SIMULATION-II, COMBINATIONAL LOGIC DESIGN-I.
- COMBINATIONAL LOGIC DESIGN-II, COMBINATIONAL LOGIC DESIGN-III
- COMBINATIONAL LOGIC DESIGN-IV
- COMBINATIONAL LOGIC DESIGN-V, COMBINATIONAL LOGIC DESIGN-VI,
- SEQUENTIAL LOGIC DESIGN-I, SEQUENTIAL LOGIC DESIGN-II,
- SEQUENTIAL LOGIC DESIGN-III

INSTRUCTIONS

- REGISTERED STUDENT NEED TO SATISFY THE SPECIFIED TO CONDITIONS TO GET THE CERTIFICATE

CERTIFICATION REQUIREMENTS

- **MUST HAVE 80% OF ATTENDANCE**
- **MUST GOT 60% OF MARKS IN THE ASSESSMENT**

Eligibility:

THIS WORKSHOP IS INTENDED FOR UG, PG STUDENTS, BASICS OF WEB TECHNOLOGY

REGISTRATION

REGISTRATION FEE: RS. 150/- PER PARTICIPANT (INCLUDES REFRESHMENT, TRAINING AND CERTIFICATE)

ADDRESS FOR COMMUNICATION

SK MONA
COORDINATORS,
FUNDAMENTAL ALGORITHMS: DESIGN AND ANALYSIS
ESWAR ENGINEERING COLLEGE.
NARASARAOPET, PALNADU (DIST)- 522 601
E-MAIL ID: ESWAR.ECEHOD@GMAIL.COM
MOBILE :9059735487

VENUE

ECE DEPARTMENT DIGITAL CLASS ROOM NO: 120

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Palnadu Dist, A.P 522 549

Resource Persons:

J Kavitha, Associate Professor, Department of CSE, St. Anns College of Engineering and Technology, Chirala

Chief Patron:

SK MEERAVALI,
Chairman

CO-Patron:
SK KAREEM MOHIDDIN
Secretary & Correspondent

CO-Patron:
SK MASTAN SHAREEF
Managing Director

Patron:
Dr G NAGAMALLESWARA RAO
Principal

Convener:

Dr K Sanjeeva Rao
HOD, Department of ECE,

<u>Faculty Coordinator</u>

SK MONA
Assistant Professor, Department of ECE,
Eswar College of Engineering, Narasaraopet.
email: eswar.ecehod@gmail.com
Phone: 9059735487

ABOUT THE COLLEGE

ESWAR COLLEGE OF ENGINEERING has established with a motive to nuture world-class engineering graduates who can contribute to the growth of the nation with their unique skills. The college administration believes that a nation will move forward when Science & Technology flourishes in that nation and eradicates social evils through their wisdom. To reach such destination there is a need of value based quality education institutes with world-class infrastructure. Fulfilling this valuable need Shaik Dada Saheb Charitable Trust has established Eswar College of Engineering in the year 2008 on chilakaluripet road just 5KM from Narasaraopet, Guntur(DT) of Andhra Pradesh at an extent of 22 acres. The College is affiliated to JNTU-Kakinada and approved by AICTE, New Delhi.

Today, Eswar College of Engineering is one of the BEST Engineering Institution in Andhra Pradesh, reputed for its highly qualified and experienced faculty and excellent infrastructural facilities for curricular and extra curricular activities, the College has maintained an enviable academic excellence right from its inception.

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ABOUT THE DEPARTMENT

The Department of Electronics & Communication Engineering came into existence in 2001 immediately when the institute was founded. It started with an intake of 60 students which was subsequently raised to 120 over a period of time. It offers 4- a year B.Tech degree program in Electronics & Communication Engineering, 2 Year M.Tech degree in Digital Electronics and Communication system with an intake of 18.

Vision: To excel in the emerging fields of electronics and communication engineering by conducting cutting-edge research, advocating for ethical principles, and addressing societal needs

Mission:

·To provide strong fundamentals and technical skills through effective teaching learning Methodologies, disseminate knowledge by organizing seminars, field visits and workshops.

·To provide an ambiance for research through collaborations with industry and academia.

·To develop responsible citizens and professional leaders with high ethical and moral values, who contribute in dissemination of universal science and technology.

VALUE ADDED COURSE ON CMOS DIGITAL VLSI DESIGN

18-07-2022 TO 23-07-2022

ORGANIZED BY DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING.

ESWAR COLLEGE OF ENGINEERING
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PALNADU DIST. A.P.
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AFFILIATED TO JNTU,KAKINADA

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Proposed Syllabus and schedule

Day 1:

Morning Session:

Introduction to CMOS Digital VLSI Design

Lecture 1 (1.5L): Overview of CMOS Technology and its Advantages

Lecture 2 (1.5L): Basics of VLSI Design and its Importance.

Afternoon Session:

CMOS Inverter Design

Lecture 3 (1.5L): Introduction to CMOS Inverter and its Operation.

Lecture 4 (1.5L): CMOS Inverter Design: Static Characteristics and DC Analysis.

Day 2:

Morning Session:

CMOS Logic Gates

Lecture 5 (1.5L): Design and Analysis of CMOS NAND and NOR Gates.

Lecture 6 (1.5L): Design and Analysis of CMOS AND, OR, and XOR Gates.

Afternoon Session:

CMOS Transmission Gates and Pass Transistors

Lecture 7 (1.5L): Introduction to CMOS Transmission Gates and Pass Transistors.

Lecture 8 (1.5L): Design and Analysis of CMOS Transmission Gates and Pass Transistors.

Day 3:

Morning Session:

CMOS Flip-Flops and Latches

Lecture 9 (1.5L): Introduction to CMOS Flip-Flops and Latches.

Lecture 10 (1.5L): Design and Analysis of CMOS D Flip-Flop and SR Latch.

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CO Statements

CO's	CO Statements
CO1	Understand MOS transistor basics, analyze their parameters, and apply knowledge to simple electronic circuit design.
CO2	Demonstrate proficiency in CMOS inverter design, grasp combinational logic principles, and design circuits using SPICE simulation.
CO3	Gain hands-on experience with SPICE simulation tools, comprehend power analysis in electronic circuits, and apply techniques for circuit optimization.
CO4	Explore advanced combinational logic design topics, develop skills in designing complex logic circuits, and optimize performance for specific applications.
CO5	Master the principles of CMOS Parasitic & SPICE Model, and understand the fundamentals of CMOS Inverter operation and optimization.
CO6	Enhance skills in combinational logic design, analyze and optimize logic circuits using systematic methodologies, and apply SPICE simulation for validation.

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Schedule

Day 1		
Morning session	Overview of CMOS Technology and its Advantages, Basics of VLSI Design and its Importance.	3 Hrs
Afternoon session	Introduction to CMOS Inverter and its Operation, CMOS Inverter Design: Static Characteristics and DC Analysis	3 Hrs
Morning session	Design and Analysis of CMOS NAND and NOR Gates, Design and Analysis of CMOS AND, OR, and XOR Gates	3Hrs
Afternoon session	Introduction to CMOS Transmission Gates and Pass Transistors, Design and Analysis of CMOS Transmission Gates and Pass Transistors	3Hrs
Day 3		
Morning session	Design of CMOS Multiplexers and Demultiplexers, Design of CMOS Adders and Subtractors	3Hrs
Afternoon session	Introduction to CMOS Flip-Flops and Latches, Design and Analysis of CMOS D Flip-Flop and SR Latch.....	3Hrs
Day 4		
Morning session	**CMOS Sequential Circuit Design** Design of CMOS Counters and Shift Registers, Design of CMOS Memory Elements: SRAM and DRAM.	3Hrs
Afternoon session	**CMOS Circuit Simulations and Layout** Introduction to CMOS Circuit Simulations. Basics of CMOS Layout Design and Fabrication Processes	3Hrs
Day 5		
Morning session	**CMOS Scaling and Technology Trends** Introduction to CMOS Scaling and Moore's Law, Advanced CMOS Technologies: FinFET and beyond	3Hrs
Afternoon session	**CMOS Power Dissipation and Low-Power Design** Sources of Power Dissipation in CMOS Circuits, Low-Power Design Techniques in CMOS VLSI	3Hrs
Day 6		
Morning session	**CMOS Testing and Verification** Introduction to CMOS Testing and Testability, CMOS Verification Techniques: Simulation and Formal Verification	3Hrs
Afternoon session	**CMOS Memory Design** Introduction to CMOS Memory Design: ROM and Flash Memory, Design and Analysis of CMOS Dynamic Memory Cells	3Hrs

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Department of Electronics and Communication Engineering

Feedback form

Course Name: CMOS Digital VLSI Design

Please place tick marks at the respective column

S.No	Particulars	Excellent	Very good	Good	Average	Poor
1	How well did you achieve this learning goal in this course?	✓				
2	Does the course contain meet the expectation?		✓			
3	Is The lecture sequence was well planned	✓				
4	Does the Lecture content illustrate with adequate examples	✓				
5	Do you Level of the course up to the standards?		✓			
6	Does the Course meets the level of new knowledge		✓			
7	Is th lecture clear and easy to understand?	✓				
8	Did your expect Teaching aids are effectively used?		✓			
9	Does the resource person interacted well and cleared the doubts.	✓				
10	Overall organization of the course		✓			

Comments

1. we learn about the design and Analysis of NAND and NOR Gates
2.

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J. Hemalatha
Signature of the student

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Department of Electronics and Communication Engineering

Feedback form

Course Name: CMOS Digital VLSI Design

Please place tick marks at the respective column

S.No	Particulars	Excellent	Very good	Good	Average	Poor
1	How well did you achieve this learning goal in this course?	✓				
2	Does the course contain meet the expectation?	✓				
3	Is The lecture sequence was well planned		✓			
4	Does the Lecture content illustrate with adequate examples	✓				
5	Do you Level of the course up to the standards?		✓			
6	Does the Course meets the level of new knowledge		✓			
7	Is th lecture clear and easy to understand?	✓				
8	Did your expect Teaching aids are effectively used?	✓				
9	Does the resource person interacted well and cleared the doubts.		✓			
10	Overall organization of the course	✓				

Comments

1. we learn about introduction to cmos inverter and operation
2. we learn about cmos inverter design: static characteristics and DC Analysis.

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P. manisai
Signature of the student

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Department of Electronics and Communication Engineering

Feedback form

Course Name: CMOS Digital VLSI Design

Please place tick marks at the respective column

S.No	Particulars	Excellent	Very good	Good	Average	Poor
1	How well did you achieve this learning goal in this course?		✓			
2	Does the course contain meet the expectation?	✓				
3	Is The lecture sequence was well planned	✓				
4	Does the Lecture content illustrate with adequate examples	✓				
5	Do you Level of the course up to the standards?		✓			
6	Does the Course meets the level of new knowledge	✓				
7	Is th lecture clear and easy to understand?		✓			
8	Did your expect Teaching aids are effectively used?	✓				
9	Does the resource person interacted well and cleared the doubts.	✓				
10	Overall organization of the course		✓			

Comments

1. We learn about Introduction to CMOS transmition gates and pass transistors

2.

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B. Mallikarjuna
Signature of the student

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9121214708

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Department of Electronics and Communication Engineering

Feedback Analysis

Course Name: CMOS DIGITAL VLSI DESIGN

Number of students attended/ given feedback 106

S.No	Particulars	Excellent	Very good	Good	Average	Poor	levels
1	How well did you achieve this learning goal in this course?	60	25	20	1		0.839622642
2	The course contain meet the expectation	66	20	20			0.858490566
3	The lecture sequence was well planned	62	24	15	2	3	0.830188679
4	Lecture content illustrated with adequate examples	65	20	20	1		0.851415094
5	Level of the course up to the mark?	66	20	20			0.858490566
6	Course highlights the level of new knowledge	60	30	10	3	3	0.83254717
7	The lecture was clear and easy to understand?	63	23	15	5		0.839622642
8	Teaching aids are effectively used?	69	20	15	2		0.867924528
9	The resource person interacted well and cleared the doubts.	70	20	15	1		0.875
10	Overall organization of the course	70	25	10	1		0.886792453
							0.854009434

Over all feedback value :	3.41603774

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Evaluation of the Value-Added Courses

Answer all the Questions Each Question Carry 1 Mark

Total Marks: 20M **Min Marks: 12 Marks**

Name of the Student **H.T.No:** **Marks obtained:**

1. What is the primary function of a MOS transistor? [b]

a) Amplification **b) Digital switching** c) Power regulation d) Signal modulation

2. Which parameter is NOT typically associated with MOS transistor characteristics? [c]

a) Threshold voltage b) Drain current **c) Inductance** d) Gate capacitance

3. What does CMOS stand for? [b]

a) Complex Metal-Oxide Semiconductor **b) Complementary Metal-Oxide Semiconductor**

c) Continuous Metal-Oxide Semiconductor d) Conductor Metal-Oxide Semiconductor

4. What is SPICE used for in electronic circuit design? [c]

a) Digital logic synthesis b) Power analysis **c) Circuit simulation** d) PCB layout

5. Which tool is commonly used for analyzing and optimizing power consumption in circuits?

a) SPICE simulation b) CMOS inverter design [d]

c) MOS transistor modelling **d) Power analysis software**

6. What is the primary purpose of a CMOS inverter? [c]

a) Voltage amplification b) Current regulation **c) Logic inversion** d) Signal attenuation

7. In a CMOS inverter, when the input is high, the output is: [a]

a) Low b) High c) Floating d) Oscillating

8. Which type of logic design involves no feedback loops? [a]

a) Combinational logic b) Sequential logic c) Asynchronous logic d) Synchronous logic

9. What does a SPICE model primarily represent? [b]

a) Physical layout of a circuit **b) Mathematical model of circuit behavior**

c) Circuit manufacturing process d) Circuit documentation

10. What is the primary purpose of MOS parasitic modeling? [c]

a) Enhance digital switching speed b) Minimize power consumption

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c) Analyze unwanted effects in MOS transistors d) Increase thermal efficiency

11. In CMOS technology, what does the 'C' stand for? [a]

a) Complementary b) Capacitive c) Conduction d) Continuous

12. What is the primary objective of power analysis in electronic circuits? [c]

a) Increase circuit speed b) Minimize circuit size

c) Optimize power consumption d) Maximize voltage levels

13. Which of the following is NOT a typical component of a CMOS inverter? [c]

a) NMOS transistor b) PMOS transistor **c) Inductor** d) Capacitor

14. What is the primary advantage of using CMOS technology? [d]

a) High power consumption b) Slow switching speed

c) Low power consumption d) Limited voltage range

15. What does the SPICE tool primarily simulate? [b]

a) Physical circuit layout **b) Electronic component behavior**

c) Circuit fabrication process d) Signal propagation

16. Which parameter is crucial for MOS transistor operation? [d]

a) Resistance b) Capacitance c) Inductance **d) Transconductance**

17. What is the primary difference between combinational and sequential logic? [b]

a) Feedback loops **b) Time dependency**

c) Input-output relationships d) Power consumption

18. What does the 'S' in SPICE stand for? [ ]

a) System **b) Simulation** c) Synchronous d) Signal

19. Which of the following is a typical application of MOS transistors? [d]

a) Audio amplification **b) Digital logic circuits**

c) RF signal modulation d) Power generation

20. What is the primary goal of combinational logic design? [ ]

a) Signal storage b) Data synchronization

c) Logic function implementation d) Feedback control

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Evaluation of the Value-Added Courses

Key

Q.No	Answer	Q.No	Answer
1	B	11	A
2	C	12	C
3	B	13	C
4	C	14	C
5	D	15	B
6	C	16	D
7	A	17	B
8	A	18	B
9	B	19	B
10	C	20	C

Coordinator

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Evaluation of the Value-Added Courses

Answer all the Questions Each Question Carry 1 Mark

Total Marks: 20M Min Marks: 12 Marks

Name of the Student Shaik. Asifa H.T.No:19X1A0404 Marks obtained: 16

1. What is the primary function of a MOS transistor? [b]

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c) Analyze unwanted effects in MOS transistors d) Increase thermal efficiency

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a) Physical circuit layout b) Electronic component behavior

c) Circuit fabrication process d) Signal propagation

16. Which parameter is crucial for MOS transistor operation? [d]

a) Resistance b) Capacitance c) Inductance d) Transconductance

17. What is the primary difference between combinational and sequential logic? [b]

a) Feedback loops b) Time dependency

c) Input-output relationships d) Power consumption

18. What does the 'S' in SPICE stand for? [b]

a) System b) Simulation c) Synchronous d) Signal

19. Which of the following is a typical application of MOS transistors? [d]

a) Audio amplification b) Digital logic circuits

c) RF signal modulation d) Power generation

20. What is the primary goal of combinational logic design? [c]

a) Signal storage b) Data synchronization

c) Logic function implementation d) Feedback control

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Department of Electronics and Communication Engineering

Course Name: CMOS Digital VLSI Design

Evaluation of the Value-Added Courses

Answer all the Questions Each Question Carry 1 Mark

Total Marks: 20M Min Marks: 12 Marks

Name of the Student N. GOPI H.T.No: 19JC1A0417 Marks obtained: 13

1. What is the primary function of a MOS transistor? [b]

a) Amplification b) Digital switching c) Power regulation d) Signal modulation

2. Which parameter is NOT typically associated with MOS transistor characteristics? [c]

a) Threshold voltage b) Drain current c) Inductance d) Gate capacitance

3. What does CMOS stand for? [b]

a) Complex Metal-Oxide Semiconductor b) Complementary Metal-Oxide Semiconductor

c) Continuous Metal-Oxide Semiconductor d) Conductor Metal-Oxide Semiconductor

4. What is SPICE used for in electronic circuit design? [a]

a) Digital logic synthesis b) Power analysis c) Circuit simulation d) PCB layout

5. Which tool is commonly used for analyzing and optimizing power consumption in circuits?

a) SPICE simulation b) CMOS inverter design [b]

c) MOS transistor modelling d) Power analysis software

6. What is the primary purpose of a CMOS inverter? [c]

a) Voltage amplification b) Current regulation c) Logic inversion d) Signal attenuation

7. In a CMOS inverter, when the input is high, the output is: [d]

a) Low b) High c) Floating d) Oscillating

8. Which type of logic design involves no feedback loops? [a]

a) Combinational logic b) Sequential logic c) Asynchronous logic d) Synchronous logic

9. What does a SPICE model primarily represent? [b]

a) Physical layout of a circuit b) Mathematical model of circuit behavior

c) Circuit manufacturing process d) Circuit documentation

10. What is the primary purpose of MOS parasitic modeling? [c]

a) Enhance digital switching speed b) Minimize power consumption

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c) Analyze unwanted effects in MOS transistors d) Increase thermal efficiency

11. In CMOS technology, what does the 'C' stand for? [a]

a) Complementary b) Capacitive c) Conduction d) Continuous

12. What is the primary objective of power analysis in electronic circuits? [c]

a) Increase circuit speed b) Minimize circuit size

c) Optimize power consumption d) Maximize voltage levels

13. Which of the following is NOT a typical component of a CMOS inverter? [c]

a) NMOS transistor b) PMOS transistor c) Inductor d) Capacitor

14. What is the primary advantage of using CMOS technology? [d]

a) High power consumption b) Slow switching speed

c) Low power consumption d) Limited voltage range

15. What does the SPICE tool primarily simulate? [b]

a) Physical circuit layout b) Electronic component behavior

c) Circuit fabrication process d) Signal propagation

16. Which parameter is crucial for MOS transistor operation? [d]

a) Resistance b) Capacitance c) Inductance d) Transconductance

17. What is the primary difference between combinational and sequential logic? [b]

a) Feedback loops b) Time dependency

c) Input-output relationships d) Power consumption

18. What does the 'S' in SPICE stand for? [b]

a) System b) Simulation c) Synchronous d) Signal

19. Which of the following is a typical application of MOS transistors? [a]

a) Audio amplification b) Digital logic circuits

c) RF signal modulation d) Power generation

20. What is the primary goal of combinational logic design?

a) Signal storage b) Data synchronization

c) Logic function implementation d) Feedback control

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Department of Electronics and Communication Engineering

Marks sheet

1 Week Add-On Course on "CMOS Digital VLSI Design"

Date: 18-07-2022 to 23-07-2022.

S.No.	HT.NO	Student Name	Marks
1	19JE1A0401	PULIBANDLA AKANKSHA DIVYASRI	15
2	19JE1A0403	REDDY ANUSHA	14
3	19JE1A0404	SHAIK ARIFA	16
4	19JE1A0405	DHARANIKOTA ASHOK KUMAR	13
5	19JE1A0406	SHAIK ASIFA	15
6	19JE1A0407	SHAIK ASMA	13
7	19JE1A0408	SHAIK BAJI BABA	13
8	19JE1A0409	RACHUMALLU BHAGYA LAKSHMI	14
9	19JE1A0410	KUNAPAREDDY BHASKAR	16
10	19JE1A0412	SHAIK CHANDINI MUBEENA	15
11	19JE1A0413	CHIMATA CHANDRIKA	16
12	19JE1A0414	MULLAMURI DEEPIKA	13
13	19JE1A0415	EEPI DEVA KALYAN	16
14	19JE1A0416	SHAIK GHOUSE JILANI	12
15	19JE1A0417	NANABALA GOPI	13
16	19JE1A0418	YENIGANDLA GOPI LAKSHMI NARASIMHA RAO	14
17	19JE1A0419	SHAIK GOUSYA DILKUSH	13
18	19JE1A0420	TAMATAM GOVINDA REDDY	12
19	19JE1A0421	ATCHULA HARIKA	15
20	19JE1A0422	KOTHURI HARITHA	17
21	19JE1A0423	CHINNAPUREDDY HEMA PRIYA	12
22	19JE1A0424	TALLAPOGU HEMANTH ROY	13
23	19JE1A0425	SHAIK JABEEN	12

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24	19JE1A0426	BATTULA JYOTHI	13
25	19JE1A0427	DUDDEMPUDI KALYAN	13
26	19JE1A0428	AMAROJU KAMESHWARAO	12
27	19JE1A0429	SHAIK KARIMULLA	12
28	19JE1A0430	DASARI KARTHIK	12
29	19JE1A0431	GUNTAKA KASI REDDY	13
30	19JE1A0432	KAMMA KAVYA	14
31	19JE1A0433	SHAIK KHAJAVALI	12
32	19JE1A0434	GOGULAMUDI KRISHNA REDDY	15
33	19JE1A0435	SANJIVI KUMARA SURYA RAKESH	14
34	19JE1A0437	SHAIK LATTI SAIDA	13
35	19JE1A0438	BANKA LAVANYA	14
36	19JE1A0439	NUTHALAPATI LEELA SAHITHI	13
37	19JE1A0440	SHAIK MAHABOOB KHALEETH	12
38	19JE1A0441	JANGILI MAHANTHI	12
39	19JE1A0442	ATINA MAHESH BABU	15
40	19JE1A0443	BASTIPATI MALLIKARJUNA	15
41	19JE1A0444	PAPANA MANISAI	13
42	19JE1A0445	MADDIRALA MERSI	14
43	19JE1A0446	SYED MOHAMMAD GULAM SAROOR	12
44	19JE1A0447	SHAIK MOHAMMAD RAFI	13
45	19JE1A0448	SHAIK MOHAMMAD RAFI	13
46	19JE1A0449	CHATTU MOUNIKA LAKSHMI	12
47	19JE1A0450	THIMMAREDDY NARAYANA REDDY	14
48	19JE1A0451	MEKALA NARESH	13
49	19JE1A0452	NASEEMA SHAIK	13
50	19JE1A0453	KALLAM NAVEEN	13
51	19JE1A0454	MUPPALLA NIKHILA	12
52	19JE1A0455	VIDADALA P N VENKATESH	12
53	19JE1A0457	CHILAKALA PRAKASHREDDY	12
54	19JE1A0458	BATTULA PRASANTHI	13
55	19JE1A0459	NELLURI PRAVALLIKA	13
56	19JE1A0460	BATTU PRAVALLIKA	12

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57	19JE1A0461	VALLEPU PRIYANKA	15
58	19JE1A0462	NAKKA RAMA KRISHNA	12
59	19JE1A0463	YENDLURI RAMYA SRI	13
60	19JE1A0464	UPPALAPATI RATHNA KOTESWARI	17
61	19JE1A0465	DAVULURI RAVI TEJA	15
62	19JE1A0466	SHAIK RESHMA	17
63	19JE1A0467	PATHAN RIZWANA	16
64	19JE1A0468	KANDRU SAI DEEPA	15
65	19JE1A0469	THOTA SAI KRISHNA	15
66	19JE1A0470	KAMISETTY SAI LAKSHMI PRASANNA	15
67	19JE1A0472	DUSI SAIKRISHNA	17
68	19JE1A0473	SYED SALIMA	15
69	19JE1A0474	SHAIK SANA SULTHANA	13
70	19JE1A0475	SHAIK SHAKIRA	12
71	19JE1A0476	PITCHALA SHALEM RAJA REDDY	12
72	19JE1A0477	SHAIK SHARMILA BEGAM	12
73	19JE1A0479	MALLA SOWJANYA	12
74	19JE1A0480	DURBAKULA SRINIVASA RAO	17
75	19JE1A0481	SHAIK SUMERA	13
76	19JE1A0482	POGIRI SUNIL KUMAR	13
77	19JE1A0483	GUDURI SURESH	12
78	19JE1A0484	JAMALLAMUDI SUVARNA	13
79	19JE1A0485	BALUSUPATI TEJASRI	13
80	19JE1A0486	KOMATINENI TEJESWARI	14
81	19JE1A0487	GANTA THIRUPATHI RAO	13
82	19JE1A0488	AAKULA TRIVENI	13
83	19JE1A0489	SAYYAD UMAR FAROOK	12
84	19JE1A0490	THAMMISETTI VAISHNU	14
85	19JE1A0491	MARTHA VAMSI	13
86	19JE1A0492	THUMMALAPALLI VASANTHI	16
87	19JE1A0493	KALYANAM VASAVI MANORAMA	15
88	19JE1A0494	VEERABABU PASUPULETI	14
89	19JE1A0495	INKOLLU VENKAT BHARGAV	16

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90	19JE1A0496	DEVALLA VENKATA ANJANEYULU	15
91	19JE1A0498	BANALA VENKATESH	14
92	19JE1A0499	VELPULA VENKATESH	16
93	19JE1A04A0	MUDENNA VENKATESWARLU	12
94	19JE1A04A1	BATHULA VENKAYAMMA	14
95	19JE1A04A2	PAGIDIPALLI VIJAYA	13
96	19JE1A04A3	AKURATHI YAMUNA	13
97	19JE1A04A4	SRINIVASAN G	14
98	20JE5A0401	DANDEBOINASRIDEVI	13
99	20JE5A0402	GUNDA AMARA RAMABRAHMASURENDRA	12
100	20JE5A0403	KAKUMANUSRILAKSHMI	16
101	20JE5A0404	KOTA MOHANAPRIYANKA	17
102	20JE5A0405	MOGALASMA	12
103	20JE5A0406	PENDELA VENKATA RAMAKRISHNA	13
104	20JE5A0407	SAKE UMA MAHESWARA RAO	12
105	20JE5A0408	SHAIK JANIBABU	16
106	20JE5A0409	SIDDULA RAMA SAILESH	18

Course Coordinator
SHAIK. MONA

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Department of Electronics and Communication Engineering

Summary of the Program

Course Name: CMOS Digital VLSI Design

The Department of Electronics and Communication Engineering at Eswar College of Engineering, Narasaraopet, proposes to conduct a one-week value-added course on " **CMOS Digital VLSI Design** from **18-07-2022 to 23-07-2022**. The course aims to enhance the skills and knowledge of 106 students from IV B.Tech I Sem ECE-A.

Evaluation Criteria for Certification:

- Marks: Students were required to secure a minimum of 60% marks in the evaluation.
- Attendance: A minimum of 80% attendance was mandatory for certification.

Objectives of the Course:

Understanding MOS Transistors: Students were introduced to the basics of MOS transistors, their parameters, and their application in electronic circuit design.

CMOS Inverter Design: The course covered the fundamentals of CMOS inverter design, CMOS parasitic elements, and SPICE modeling to understand CMOS inverter operation and optimization.

Power Analysis and SPICE Simulation: Students learned power analysis techniques in electronic circuits and gained hands-on experience with SPICE simulation tools for circuit validation and optimization.

Combinational Logic Design: The course delved into advanced topics of combinational logic design, enabling students to design, analyze, and optimize complex logic circuits using systematic methodologies.

Course Delivery Method:

- The course consisted of lectures, and practical sessions, conducted by **Dr. V Praveen**, an experienced faculty member from the Department of CSE.
- Interactive sessions encouraged active participation and engagement from the students to ensure effective learning and understanding of the concepts.

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Benefits for Students:

Enhanced Technical Skills: The course equips students with comprehensive knowledge and practical skills in CMOS digital VLSI design, enhancing their technical proficiency in electronics and communication engineering.

Career Readiness: By mastering essential concepts and tools like SPICE simulation and combinational logic design, students are better prepared for advanced studies and lucrative career

opportunities in the semiconductor industry, electronic design automation, and research and development sectors.

Practical Experience: Through hands-on experience with SPICE simulation tools and real-world design projects, students gain valuable practical experience, enabling them to tackle real-world challenges and contribute effectively to innovative electronic design projects and research initiatives.

In conclusion, the "CMOS Digital VLSI Design" course has been instrumental in empowering students with the knowledge, skills, and confidence required to navigate and contribute effectively to the rapidly evolving field of electronic design and VLSI technology.

Faculty Coordinator

HOD-ECE

Principal

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